AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An integrated circuit structure comprising:

a semiconductor layer having a major surface formed along a plane;

first and second spaced-apart doped regions extending into the surface from the plane;

a monocrystalline third doped region of different conductivity type than the first region, positioned above the plane and over the first region; and

a conductive layer [formed] between the first and second regions and above the plane, providing electrical connection between the doped regions[.], wherein the conductive layer comprises one or more materials taken from the group comprising tungsten silicide, tungsten nitride, titanium silicide, titanium nitride and cobalt silicide.

2. (Original) The structure of claim 1 wherein the first doped region is a first source/drain region of a MOSFET and the third region is a channel region of the MOSFET.

3. (Original) The structure of claim 2 wherein the second region is a portion of a transistor.

4. (Original) The structure of claim 2 wherein the second region is a second source/drain region associated with a second MOSFET, said structure further comprising a channel region of the second MOSFET aligned with the second source/drain region.

5. (Original) The structure of claim 1 further including:

a fourth doped region over the second region of different conductivity type than the second region;

a fifth doped region over the fourth doped region of the same conductivity type as the second region;

a sixth doped region over the third doped region of the same conductivity type as the first region, said first, second, third, fourth, fifth and sixth regions and conductive layer configured as two interconnected transistors.

6. (Original) The structure of claim 5 wherein the two transistors are of complementary conductivity type.

7. (Original) The structure of claim 5 wherein one of the transistors is a MOSFET.

8. (Original) The structure of claim 5 wherein the transistors are configured to form an inverter circuit.

9. (Previously Amended) An integrated circuit structure comprising:

a semiconductor layer having a major surface formed along a plane;

first and second spaced-apart doped regions formed in the surface;

a third doped region over the first region of different conductivity type than the first region; and

a conductive layer formed between the first and second regions and above the plane, providing electrical connection between the doped regions, wherein the conductive layer comprises one or more materials taken from the group comprising tungsten silicide, tungsten nitride, titanium silicide, titanium nitride and cobalt silicide.

10. (Previously Amended) The structure of claim 1 wherein the doped regions are configured to form an inverter circuit.

11. (Original) The structure of claim 1 wherein the first and second doped regions are first and second source/drain regions and the third region is a channel region, said structure further comprising:

a second channel region formed over the second source/drain region;

third and fourth spaced-apart source/drain regions each vertically aligned with one of the channel regions and one of the first and second source/drain regions; and

a conductive element connected to simultaneously control operation of both transistors.

12. (Original) The structure of claim 11 wherein the conductive element comprises polysilicon and the transistors each include a gate contact region adjacent the channel

region and connected to the conductive element, said transistors configured to form an inverter circuit function.

13. (Original) The structure of claim 1 wherein the conductive layer is a continuous film extending from the first region to the second region.

14. (Original) The structure of claim 1 wherein the conductive layer physically contacts the first region and the second region.

15. (Previously Amended) A semiconductor device comprising:

a first layer of semiconductor material;

a first field effect transistor having a first source/drain region formed in the first layer, a channel region formed over the first layer and a second source/drain region formed over the channel region;

a second field effect transistor having a first source/drain region formed in the first layer, a channel region formed over the first layer and a second source/drain region formed over the channel region; and

a conductive layer in a plane extending between the first layer and the first field effect transistor channel region, said conductive layer comprising a metal positioned between the first source/drain region of each transistor to conduct current from one first source/drain region to the other first source/drain region.

16. (Original) The device of claim 15 wherein the first and second transistors are connected to form a circuit.

17. (Original) The device of claim 15 comprising a plurality of additional field effect transistors each having a first source/drain region formed in the first layer, a channel region formed over the first layer and a second source/drain region formed over the channel region, the first, second and additional transistors configured into a circuit.

18. (Original) The device of claim 17 wherein four of the additional transistors are connected with the first and second transistors to form an SRAM circuit cell.

19. (Previously Amended) A semiconductor device comprising:

a first layer of semiconductor material;

a first field effect transistor having a first source/drain region formed in the first layer, a channel region formed over the first layer and a second source/drain region formed over the channel region;

a second field effect transistor having a first source/drain region formed in the first layer, a channel region formed over the first layer and a second source/drain region formed over the channel region; and

a conductive layer comprising a metal positioned between the first source/drain region of each transistor to conduct current from one first source/drain region to the other first source/drain region, wherein the conductive layer comprises a metal silicide.

20 -31 (Previously Cancelled)